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EXAMINER	
LEE, CHEUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/765,393	CAMPBELL, KRISTY A.
	Examiner	Art Unit
	Cheung Lee	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *61-82,84-89,91-109,111-119 and 144-148* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *61-82,84-89,91-109,111-115 and 144-148* is/are rejected.

7)☒ Claim(s) *116-119* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. Applicant's Amendment and Response to the Office Action mailed on August 9, 2005 has been entered and made of record.

Response to Amendments

2. In view of Applicant's amendments and arguments filed on January 9, 2006, the rejections of claims 61-83, 84-89, 91-109 and 111-119 under 35 U.S.C. 102(b), 102(e) or 103(a), as stated in the indicated Office Action, have been withdrawn. Applicant's arguments have been rendered moot in view of the new or modified ground of rejection given below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 99 and 113-116 are rejected under 35 U.S.C. 102(e) as being anticipated by Campbell et al. (US Pub. 2004/0042259; hereinafter "Campbell").

4. With respect to claim 99, referring to figures 1-2, Campbell discloses a method of forming a memory element (page 2, paragraph 22; fig. 1), said method comprising: forming at least one chalcogenide glass layer 17 (page 2, paragraph 26); forming at least one metal-containing layer 18 over said chalcogenide glass layer; forming a second metal containing layer 118 over the first metal-containing layer; electrically coupling first 14 and second electrodes 22 to said chalcogenide glass layer (page 4, paragraph 43; see claims 54 and 60); and applying a conditioning pulse to the memory element to bond regions of metal and glass within said chalcogenide glass layer (page 1, paragraphs 3-6; page 2, paragraph 27), said bonded regions forming at least one conducting channel within said chalcogenide glass layer (page 1, paragraphs 3-5). Campbell discloses usage of germanium-selenide glass doped with silver for resistance variable material, the examiner takes the position that the step of forming a conducting channel or a dendrite within the resistance variable material under the influence of the applied voltage is inherently performed (page 1, paragraphs 3-5).

5. With respect to claim 113, Campbell discloses wherein further comprising forming a second chalcogenide glass layer 117 over said at least one metal-containing layer 18.

6. With respect to claim 114, Campbell discloses wherein said second chalcogenide glass layer is from about 100 Å to about 300 Å thick (pages 2 and 3, paragraph 32).

7. With respect to claim 115, Campbell discloses wherein further comprising forming a second metal-containing layer 118 over said second chalcogenide glass layer 117.

8. Claims 145-148 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozicki (US Pub. 2003/0137869).

9. With respect to claim 145, referring to figures 1-14, Kozicki discloses a method of forming a memory element 100, said method comprising: forming at least one chalcogenine glass layer 140 (page 6, paragraph 60); forming at least one $Ag_{2+x}Se$ layer 155 (page 5, paragraph 53) over said chalcogenide glass layer; and applying a conditioning voltage to the memory element (page 3, paragraph 39) sufficient to cause Ag_2Se molecules to enter into said chalcogenide glass layer (page 5, paragraph 56) and bond with molecules of said chalcogenide glass layer (page 6, paragraphs 64-65).

10. With respect to claim 146, Kozicki discloses wherein said step of applying a conditioning voltage to sufficient to cause Ag_2Se molecules to bond with molecules of the said chalcogenide glass layers forms at least one conductive channel 160 (page 3, paragraph 39).

11. With respect to claim 147, Kozicki discloses wherein said chalcogenide glass layer has a stoichiometry of Ge_xSe_{100-x} (page 6, paragraphs 60, 63 and 65).

12. With respect to claim 148, Kozicki discloses wherein said $Ag_{2+x}Se$ layer may be a layer comprised of Ag_2Se molecules (page 5, paragraph 53; page 6, paragraph 65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 61-82, 84-89, 91-109, 111-112 and 144 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozicki (US Pub. 2003/0137869).

14. With respect to claim 61, referring to figures 1-14, Kozicki discloses a method of forming a memory element 100, said method comprising: forming at least one resistance variable material layer 140; forming at least one metal-containing layer 155 adjacent said resistance variable material; and forming at least one conducting channel 160 within said resistance variable material layer by applying a conditioning voltage to the memory element (page 3, paragraph 39), but Kozicki does not disclose expressly wherein said conditioning voltage has a pulse duration of from 10 to 500 ns and is approximately 700 mV or greater. However, any variation in pulse duration and voltages for conditioning voltage in the present claim is obvious in light of the cited art, because the changes in pulse duration and voltages for conditioning voltage produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

15. With respect to claim 89, referring to figures 1-14, Kozicki discloses a method of forming a memory element 100, said method comprising: forming at least one doped chalcogenide glass layer 140 (page 6, paragraph 60) with polarizable metal-chalcogen regions 306 within a glass backbone (page 6, paragraph 65), wherein said polarizable

metal-chalcogen regions are silver-selenide regions (page 6, paragraph 65); electrically coupling first 120 and second electrodes 130 to said doped chalcogenide glass layer (page 8, paragraph 85); and polarizing said metal-chalcogen regions with a conditioning voltage applied to said electrodes to form at least one conducting channel 160 comprising said polarized metal-chalcogen regions (page 3, paragraph 39; page 6, paragraph 66), the examiner takes the position that the step of becoming polarized silver selenide regions under the influence of the applied voltage is inherent due to the presence of an electric field caused by the applied voltage, but Kozicki does not disclose expressly wherein said conducting channel configured to receive and expel metal ions in response to write and erase voltages applied to said memory element. However, Kozicki discloses an electrodeposit in a write operation (page 8, paragraph 85), and also discloses wherein reversing a bias applied during the write operation in an erase operation (page 9, paragraph 92). And a conducting channel is formed by applying a conditioning voltage (page 3, paragraph 39; page 8, paragraph 85). Therefore, it would have been obvious that the steps of receiving and expelling metal ions are performed when write and erase voltages are applied via conducting channel.

16. Withrespect to claim 99, referring to figures 1-14, Kozicki discloses a method of forming a memory element 100, said method comprising: forming at least one chalcogenide glass layer 140 (page 6, paragraph 60); forming at least one metal-containing layer 155 over said chalcogenide glass layer; forming a second metal-containing layer 120 over the first metal-containing layer; electrically coupling first 120 and second electrodes 130 to said chalcogenide glass layer (page 8, paragraph 85);

and applying a conditioning voltage to the memory element (page 3, paragraph 39) to bond regions of metal and glass within said chalcogenide glass layer (page 6, paragraphs 65-66), said bonded regions forming at least one conducting channel 160 within said chalcogenide glass layer (page 3, paragraph 39; page 6, paragraphs 65-66), but Kozicki does not disclose expressly wherein applying a conditioning pulse. However, Kozicki discloses wherein a relative volatility of the memory structures can be altered by applying different amounts of energy, such as current pulse (page 8, paragraph 87). Since Kozicki does not disclose wherein applying either a constant or pulsed bias to the memory element, it would have been obvious that a voltage pulse can be applied to the memory element.

17. With respect to claim 144, referring to figures 144, Kozicki discloses a method of forming a memory element 100, said method comprising: forming at least one resistance variable material layer 140; forming at least one metal-containing layer 155 over said resistance variable material layer; and forming at least one conducting channel 160 within said resistance variable material layer by applying a conditioning voltage to the memory element (page 3, paragraph 39), but Kozicki does not disclose expressly wherein said at least one conducting channel receives an expels conductive ions upon application of a programming voltages to said resistance variable material layer. However, Kozicki discloses an electrodeposit in a write operation (page 8, paragraph 85), and also discloses wherein reversing a bias applied during the write operation in an erase operation (page 9, paragraph 92). And a conducting channel is formed by applying a conditioning voltage (page 3, paragraph 39; page 8, paragraph

85). Therefore, it would have been obvious that the steps of receiving and expelling metal ions are performed when write and erase voltages are applied via conducting channel.

18. With respect to claim 62, Kozicki discloses wherein said resistance variable material layer is a chalcogenide glass layer (pages 5-6, paragraphs 59-60).

19. With respect to claim 63, Kozicki discloses wherein said chalcogenide glass layer has a stoichiometry of Ge_xSe_{100-x} (page 6, paragraphs 60, 63 and 65).

20. With respect to claims 64, 77, 91 and 100, Kozicki does not disclose expressly wherein said doped chalcogenide glass layer has a stoichiometry from about [Claims 64 and 91] $Ge_{18}Se_{82}$ to $Ge_{25}Se_{75}$; and [Claims 77 and 100] $Ge_{20}Se_{80}$ to $Ge_{43}Se_{57}$. However, Kozicki discloses the stoichiometry of the doped chalcogenide glass layer from about $Ge_{0.17}Se_{0.83}$ to $Ge_{0.25}Se_{0.75}$ (page 6, paragraph 63). In the case where claimed ranges "overlap or lie inside rages disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F. 2d 1575, 16 USPQ 2d 1934 (Fed. Cir. 1990).

21. With respect to claim 65, Kozicki discloses wherein said chalcogenide glass layer is doped with metal ions (page 6, paragraphs 60 and 64).

22. With respect to claim 66, Kozicki discloses wherein said metal ions are silver ions (page 6, paragraph 60).

23. With respect to claims 67, 79 and 102, Kozicki does not disclose expressly wherein said doped chalcogenide glass layer is [Claim 67] from about 150 Å to about 600 Å; and [Claim 79 and 102] from about 150 Å to about 500 Å thick. However,

Kozicki discloses a thickness about 35 nanometers (page 8, paragraph 85). In the case where claimed ranges "overlap or lie inside rages disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F. 2d 1575, 16 USPQ 2d 1934 (Fed. Cir. 1990).

24. With respect to claim 68, Kozicki discloses wherein said doped chalcogenide glass layer has polarizable metal-chalcogen regions 306 (page 6, paragraph 65).

25. With respect to claim 69, Kozicki discloses wherein said polarizable metal-chalcogen regions are Ag_2Se regions within a germanium-selenide glass backbone (page 6, paragraph 65).

26. With respect to claim 70, Kozicki discloses wherein said Ag_2Se regions become aligned upon application of said conditioning voltage to said memory element (page 6, paragraph 66). Kozicki discloses wherein metal ions migrate within region 304 to bridge low-resistance regions 306 in a presence of a voltage (page 3, paragraph 39). It would have been obvious that the step of bridging low-resistance regions can also align the low-resistance regions.

27. With respect to claim 71, Kozicki discloses wherein said conditioning voltage is greater than subsequent write, read, and erase voltages (pages 8-9, paragraphs 85-92). In write operation, a voltage, which is a conditioning voltage, greater than write threshold voltage is required to form conductive region and to overcome a barrier (page 8, paragraph 85). And where no isolating barrier layer is present, an initial write threshold voltage is relatively low (page 8, paragraph 86). In read operation, a voltage, which is less than a voltage threshold, is required (page 8, paragraph 89). In erase

operation, an erase threshold voltage is much lower than a write threshold when a barrier is not present. The conditioning voltage is greater than the write threshold voltage, and the write threshold voltage is greater than read and erase threshold voltages. Thus, the conditioning voltage is greater than write, read, and erase voltages.

28. With respect to claims 72 and 92, Kozicki discloses wherein the Ag_2Se regions form at least one conducting channel by becoming polarized and aligning within the doped chalcogenide glass layer (page 6, paragraph 66). The examiner takes the position that the steps of becoming polarized and aligning silver selenide regions under the influence of the applied voltage is inherent due to the presence of an electric field caused by the applied voltage. Arguments stated in claim 70 also apply.

29. With respect to claims 73, 93 and 107, Kozicki discloses wherein prior to applying said conditioning voltage, said memory element has a first resistance state and after applying said conditioning voltage to said memory element, said memory element has a second resistance state lower than said first resistance state (page 3, paragraph 39).

30. With respect to claim 74, Kozicki discloses wherein subsequent write, read, and erase voltages have an absolute magnitude lower than that of said conditioning voltage (pages 8-9, paragraphs 85-92). Arguments stated in claim 71 also apply.

31. With respect to claims 75-76, 94-95 and 108-109, Kozicki discloses wherein [Claims 75, 94 and 108] applying a write voltage produces a third resistance state lower than the second resistance state; and [Claims 76, 95 and 109] applying a second write voltage produces a fourth resistance state lower than said third resistance state (page

8, paragraph 85; see fig. 6). Kozicki discloses an off state 610 (high-resistance state), and a low-resistance state 620 once a write step has been performed. Before applying any voltages the device is in a high resistance state, and it becomes lower resistance state after the conditioning voltage (page 3, paragraph 39). Therefore, the resistance state will keep decreasing for each write voltage. Adding up all the voltages applied in a memory element results a big change of resistant value from the first high resistant state.

32. With respect to claims 78 and 101, Kozicki does not disclose expressly wherein said chalcogenide glass layer has a stoichiometry of $Ge_{40}Se_{60}$. However, any variation in Ge-Se stoichiometry in the present claim is obvious in light of the cited art, because the changes in Ge-Se stoichiometry produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

33. With respect to claims 80 and 103, Kozicki does not disclose expressly wherein said at least one metal-containing layer is from about 300 Å to about 1200 Å thick. However, any variation in metal-containing layer's thickness in the present claim is obvious in light of the cited art, because the changes in metal-containing layer's thickness produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an

unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

34. With respect to claims 81 and 104, Kozicki discloses wherein said at least one metal-containing layer is an Ag_2Se layer (page 5, paragraph 53).

35. With respect to claim 82, Kozicki discloses wherein the conditioning voltage is applied to the memory element driving Ag_2Se into the chalcogenide glass layer (page 5, paragraph 56).

36. With respect to claims 84 and 105, Kozicki discloses wherein the chalcogenide glass layer has a germanium-selenide glass backbone (page 6, paragraphs 63 and 65).

37. With respect to claims 85 and 106, Kozicki discloses wherein the Ag_2Se bonds to the germanium-selenide glass backbone (page 5, paragraphs 53 and 56; page 6 paragraph 65) forming at least one conducting channel within said chalcogenide glass layer (page 5, paragraph 56).

38. With respect to claim 86, Kozicki discloses wherein further comprising forming a second metal-containing layer 120 over the first metal-containing layer.

39. With respect to claims 87 and 111, Kozicki discloses wherein said second metal-containing layer comprises silver ions (page 4, paragraph 44).

40. With respect to claims 88 and 112, Kozicki discloses wherein said silver ions are driven into and out of the at least one conducting channel by applying a write, erase or read voltage (page 4, paragraphs 44-45).

41. With respect to claim 96, Kozicki discloses wherein further comprising forming a metal-containing layer 155 over said doped chalcogenide glass layer (see fig. 1).

42. With respect to claim 97, Kozicki discloses wherein said metal-containing layer comprises silver (page 5, paragraph 53).

43. With respect to claim 98, Kozicki discloses wherein said metal-containing layer provides metal ions that move in and out of the conducting channel (page 5, paragraph 56).

Allowable Subject Matter

44. Claims 116-119 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: claim 116 recite said second metal containing layer is from about 100 Å to about 500 Å thick; and claims 117-119 recite forming a third metal-containing layer over said second metal-containing layer, which comprises silver ions wherein silver ions are driven into and out of the at least one conducting channel by applying a write, erase, or read voltage. These features in combination with the other elements of the claim(s) are neither disclosed nor suggested by the prior art of record.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

March 21, 2006

HA NGUYEN
PRIMARY EXAMINER